REMARKS

This Amendment responds to the Office Action dated August 2, 2005 in which the Examiner objected to the disclosure, rejected claims 1-3 under 35 U.S.C. §102(b) and rejected claim 4 under 35 U.S.C. §103.

As indicated above, the specification has been amended in order to correct a minor informality. Therefore, applicants respectfully request the Examiner approves the correction and withdraws the objection to the disclosure.

Claim 1 claims a memory device comprising a memory unit and an arbiter. The arbiter controls the memory unit while arbitrating for a bus access request from a plurality of units. When a second bus access request takes place before an access to the memory unit that corresponds to a first bus access request has been completed, the arbiter performs activation of the memory unit that corresponds to the second bus access request in parallel with the access to the memory unit that corresponds to the first bus access request.

Through the structure of the claimed invention having an arbiter which performs activation of a memory unit corresponding to a second bus access request in parallel with access to the memory unit that corresponds to a first bus access request when the second bus access request takes place before the access to the memory unit corresponding to the first bus access request has been completed, as claimed in claim 1, the claimed invention provides a memory device which does not reduce processing performance of the entire system. The prior art does not show, teach or suggest the invention as claimed in claim 1.

Claims 1-3 were rejected under 35 U.S.C. §102(b) as being anticipated by *Dreibelbis et al* (U.S. Patent No. 5,875,470).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §102(b). The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, applicants respectfully request the Examiner withdraws the rejection to the claims and allows the claims to issue.

Dreibelbis et al appears to disclose a multi-port multi-bank memory architected to enable manufacture of the memory in a single DRAM chip having a plurality of input/output ports and being capable of handling a large number of accesses in parallel. (col. 1, lines 8-12) The chip structure shown in FIGS. 1A and 1B is logically divided into distinct parts, including DRAM storage parts shown in FIG. 1A, and an input/output part shown in FIG. 1B. The storage part in FIG. 1A comprises four DRAM memory sections 1, 2, 3 and 4. Each memory section contains four DRAM storage banks connected to one data bus 5. The four storage sections 1, 2, 3, 4 each have a respective data bus 5-1, 5-2, 5-3, 5-4. The four sections therefore have a total of 16 DRAM banks 1.1 through 4.4. Further, each DRAM bank is connected to a respective one of sixteen address buses 11-1 through 14-4, which are connected to a bank address control 10 within the chip. Bank address control 10 may receive all memory addresses requested by all processors wanting to access data in any of the 16 banks in memory sections 1, 2, 3 and 4. Control 10 may be simultaneously providing plural addresses on buses 11-1 through 11-4 for simultaneously selecting the drivers for one of matrix rows in multiple banks. (col. 4, line 54 through col. 5, line 5) Only a very short time is needed for control 10 to receive an address from bus 16, and to select and transmit the address to a required bank compared to the amount of time required for that bank to access the requested row of data having that address. Consequently, bank address control 10

may receive and send many addresses to many different banks during the time that one bank is accessing data. The object of the plural memory sections is to try to maintain all banks accessing data simultaneously. This allows a synchronous timing relationship to be directly used among the different memory sections--to enable one bank in each of memory sections 1, 2, 3 and 4 to be simultaneously transferring data in either direction on the four data buses. In this embodiment, data transfers by banks in different sections start and end together during a transfer cycle sequence. For example, each bank may transfer a line of data in a sequence of four machine cycles, in which a bank in each section starts its transfer in cycle 1 and ends the transfer of the line in cycle 4. The transfer cycles may be driven by the same system clock that drives all processors in the system. There is no conflict among four simultaneous data transfers by four banks (one per memory section), since the data in each section is for an independent processor in the embodiment. Requests from the multiple processors are received by bank address control 10 which handles the requests in a first-in-first-out (FIFO) order for each processor in selecting banks for the requests. Each bank is assigned a unique range of addresses in the sequence of addresses represented in the chip memory. If a next processor request is received for a bank while it is has an active request, the next request must wait in control 10 until the required bank becomes non-busy (available), which happens when it completes its current request. (col. 5, line 57 through col. 6, line 24)

Thus, *Dreibelbis et al* merely discloses that if a next processor request is received while a bank has an active request, the next request must wait in control 10 until the required bank becomes available, which happens when it completes its current request (column 6, lines 20-24). Thus, nothing in *Dreibelbis et al* shows,

teaches or suggests that when a second bus access request takes place before a first bus access has been completed, the arbiter performs activation of the memory unit of the second bus request in parallel with the access to the memory unit of the first bus request as claimed in claim 1. Rather, *Dreibelbis et al* clearly teaches away from the claimed invention since the next request must wait until a bank becomes available.

Additionally, *Dreibelbis et al* merely discloses bank address control 10 which receives memory addresses requested by processors and simultaneously provides addresses on buses for selecting drivers of the banks. Nothing in *Dreibelbis et al* shows, teaches or suggests an arbiter which arbitrates for bus access requests as claimed in claim 1. Rather, control 10 of *Dreibelbis et al* is an address controller.

Since nothing in *Dreibelbis et al* shows, teaches or suggests an arbiter which arbitrates for bus access requests and when a second bus access request takes place before a first bus access has been completed, the arbiter performs activation of the memory unit of the second bus access request in parallel with the access of the memory unit of the first bus access request, as claimed in claim 1, applicants respectfully request the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §102(b).

Claims 2-3 depend from claim 1 and recite additional features. Applicants respectfully submit that claims 2-3 would not have been anticipated by *Dreibelbis et al* within the meaning of 35 U.S.C. §102(b) at least for the reasons as set forth above. Therefore, applicants respectfully request the Examiner withdraws the rejection to claims 2-3 under 35 U.S.C. §102(b).

Claim 4 was rejected under 35 U.S.C. §103 as being unpatentable over *Dreibelbis et al* and further in view of *Masuoka et al* (U.S. Patent No. 6,472,714).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claim has been reviewed in light of the Office Action, and for reasons which will be set forth below, applicants respectfully request the Examiner withdraws the rejection to the claim and allows the claim to issue.

As discussed above, since nothing in *Dreibelbis et al* shows, teaches or suggests the primary feature as claimed in claim 1, applicants respectfully submit that the combination of the primary reference with the secondary reference to *Masaoka et al* would not overcome the deficiencies of the primary reference. Therefore, applicants respectfully request the Examiner withdraws the rejection to claim 4 under 35 U.S.C. §103.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time.

The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BUCHANAN INGERSOLL PC

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